



Design Methodology for RF CMOS Phase Locked Loops

By Carlos Quemada

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Engineers face stiff challenges in designing phase-locked loop (PLL) circuits for wireless communications thanks to phase noise and other obstacles. This practical book comes to the rescue with a proven PLL design and optimization methodology that lets designers assess their options, predict PLL behavior, and develop cost-effective PLLs that meet performance requirements no matter what IC (integrated circuit) challenges they come up against. This uniquely comprehensive toolkit takes designers step-by-step through operation principles, design procedures, phase noise analysis, layout considerations, and Cmos realizations for each PLL building block. It provides a sample design of a fully integrated PLL for Wlan applications, demonstrating every step from specs definition and circuit characterization to layout generation and circuit schematics.

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Editorial Review

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